CLAIMS

1. A method for capturing simulation output, comprising:

providing a stimulus to a test bench;

providing a device model corresponding to an integrated circuit to the test bench; and

in response to applying the stimulus to the device model through the test bench, generating a captured simulation, the captured simulation comprising information related to at least one of strobe timing information, opcode information, mixed signal information, and internal memory content information.

2. The method of claim 1, wherein the captured simulation comprises sufficient information for automatically generating a complete test pattern within a test program corresponding to the integrated circuit.

3. The method of claim 1, wherein the captured simulation captures all communication through the test bench between the stimulus and the device model.

4. The method of claim 1, wherein the stimulus and the test bench communicate in accordance with a predetermined protocol which provides a standard interface between the stimulus and the test bench.

5. The method of claim 1, wherein the device model and the test bench communicate in accordance with a predetermined protocol which provides a standard interface between the device model and the test bench.

6. The method of claim 5, wherein all communication with the device model occurs through the standard interface between the device model and the test bench.

7. The method of claim 1, wherein the stimulus comprises verification patterns, drivers, and monitors.

8. The method of claim 7, wherein the stimulus further comprises a simulation environment corresponding to the device model.

9. The method of claim 1, wherein:

in response to applying the stimulus to the device model through the test bench, the test bench generates a plurality of simulation parameters corresponding to the stimulus and device model; and

the captured simulation is based at least in part on the simulation parameters.

10. The method of claim 1, wherein the captured simulation comprises information relating to another one of strobe timing information, opcode information, mixed signal information, and internal memory content information.

11. The method of claim 1, wherein the captured simulation further comprises information relating to at least one of directionality information, pin data information, masking information, comment information, and partial cyclized information.

12. A method for preparing a captured simulation for post-processing, comprising:

receiving the captured simulation wherein the captured simulation comprises at least one of strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to a device model through a test bench;

generating data patterns based at least in part on the one of strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools; and

providing a first formatted pattern file to a first post-processing tool, the first formatted pattern file based on the data patterns.

13. The method of claim 12, wherein the captured simulation comprises another one of strobe timing information, opcode information, mixed signal information, and internal memory content, and generating the data patterns is further based at least in part on the another one of strobe timing information, opcode information, and mixed signal information, and internal memory content information.

14. The method of claim 12, wherein the captured simulation further comprises information relating to at least one of directionality information, pin data information, masking information, comment information, and partial cyclized information.

15. The method of claim 12, wherein the data patterns include cyclized patterns.

16. The method of claim 12, wherein the first post-processing tool is one of a fault simulator, virtual tester, and automatic test equipment (ATE) tester.

17. The method of claim 16, further comprising:

providing a second formatted pattern file to a second post-processing tool, the second formatted pattern file based on the data patterns and wherein the second post-processing tool is another one of a fault simulator, virtual tester, and automatic test equipment (ATE) tester.

18. A data pattern generator stored via a computer readable medium, comprising:

a first plurality of instructions for receiving the captured simulation wherein the captured simulation comprises at least one of strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to a device model through a test bench;

a second plurality of instructions for generating data patterns based at least in part on the one of strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools; and

a third plurality of instructions for providing a first formatted pattern file to a first post-processing tool, the first formatted pattern file based on the data patterns.

19. The method of claim 18, wherein the captured simulation comprises another one of strobe timing information, opcode information, and mixed signal information, and generating the data patterns is further based at least in part on the another one of strobe timing information, opcode information, and mixed signal information.

20. The method of claim 18, wherein the first post-processing tool is one of a fault simulator, virtual tester, and automatic test equipment (ATE) tester.

21. The method of claim 20, further comprising:

a fourth plurality of instructions for providing a second formatted pattern file to a second post-processing tool, the second formatted pattern file based on the data patterns and wherein the second post-processing tool is another one of a fault simulator, virtual tester, and automatic test equipment (ATE) tester.

22. A standard reusable test bench stored via a computer readable medium, comprising:

a first plurality of instructions for receiving a stimulus;

a second plurality of instructions for receiving a device model corresponding to an integrated circuit; and

a third plurality of instructions for generating simulation parameters in response to applying the stimulus to the device model;

a fourth plurality of instructions for creating a captured simulation based at least in part on the simulation parameters, the captured simulation comprising information related to at least one of strobe timing information, opcode information, mixed signal information, and internal memory content information.

23. The method of claim 22, wherein the captured simulation comprises sufficient information for automatically generating a complete test within a test program corresponding to the integrated circuit.

24. The method of claim 22, wherein the captured simulation captures all communication between the stimulus and the device model through the standard reusable test bench.

25. The method of claim 22, wherein all communication with the device model occurs through the standard reusable test bench.

26. The method of claim 22, wherein the captured simulation comprises information relating to another one of strobe timing information, opcode information, mixed signal information, and internal memory content information.

27. The method of claim 22, wherein the captured simulation comprises information relating to at least one of directionality information, pin data information, masking information, comment information, and partial cyclized information.